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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
CHEN, ERIC BRICE

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,953	CLINE ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *18-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 12-15* is/are rejected.

7)☒ Claim(s) *3-11 and 16-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/15/04; 10/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention I, claims 1-17 in the reply filed on Aug. 11, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

2. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-2 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,380,095), in view of Flander et al. (U.S. Patent No. 6,653,734).

6. As to claim 1, Liu discloses a method for forming semiconductor structures, the method comprising the steps of: (a) forming a first plurality of deep trenches (603) (column 11, lines 24-26), wherein forming each trench of the first plurality of deep trenches includes the steps of: (i) providing a semiconductor substrate (602) (column 11, line 30; Figure 6), (ii) forming a hard mask layer (608/606/604) on top of the semiconductor substrate (602) (column 11, lines 24-27), (iii) etching a hard mask opening in the hard mask layer so as to expose the semiconductor substrate to the atmosphere through the hard mask layer opening, wherein the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening according to a first set of etching parameters (column 11, lines 45-60; column 2, lines 23-26), (iv) etching a deep trench in the substrate via the hard mask opening (column 11, lines 59-67; column 2, lines 26-29). Although Liu does not expressly disclose processing a plurality of trenches, semiconductor fabrication inherently involved the simultaneous processing of multiple devices. See Streetman, *Solid State Electronic Devices*, Prentice Hall (1990), page 332.

7. Liu does not expressly disclose Applicants' step (b). However, Liu teaches that the lateral etching of the overlying hard mask layers can cause the taper of the trench to deviate from the specified angle range (column 8, lines 47-54). Liu's first etching step is directed at protecting the hard mask layer during patterning (column 2, lines 26-29). Furthermore, Flander teaches that faceting on the walls of hard mask layer (104) can result in an undesirable enlargement of the trench to be etched (column 4, lines 47-60; Figure 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to (b) if a first yield of the first plurality of deep trenches is not within a pre-specified range of a target yield, forming a second plurality of deep trenches, wherein each trench of the second plurality of deep trenches is formed by using steps (a)(i) through (a)(iv), except that the step of etching the bottom portion of the hard mask opening is performed according to a second set of etching parameters, wherein the second set of etching parameters are adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, a side wall of the bottom portion of the hard mask opening is more vertical than that corresponding to a trench of the first plurality of deep trenches. One who is skilled in the art would be motivated to select an etching composition that produces the desired angle range, such as altering Liu's first etching step to produce a smooth hard mask layer sidewall.

8. As to claim 2, Liu does not expressly Applicants' claimed limitation. However, Liu teaches that the lateral etching of the overlying hard mask layers can cause the taper of the trench to deviate from the specified angle range (column 8, lines 47-54). Liu's first

etching step is directed at protecting the hard mask layer during patterning (column 2, lines 26-29). Furthermore, Flander teaches that faceting on the walls of hard mask layer (104) can result in an undesirable enlargement of the trench to be etched (column 4, lines 47-60; Figure 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to, if a second yield of the second plurality of deep trenches is not within the pre- specified range of a target yield, forming a third plurality of deep trenches, wherein each trench of the third plurality of deep trenches is formed by using steps (a)(i) through (a)(iv), except that the step of etching the bottom portion of the hard mask opening is performed according to a third set of etching parameters, wherein the third set of etching parameters are adjusted from the second set of etching parameters such that, for each trench of the third plurality of deep trenches, a side wall of the bottom portion of the hard mask opening is more vertical than that corresponding to a trench of the second plurality of deep trenches. One who is skilled in the art would be motivated to select an etching composition that produces the desired taper, such as altering Liu's first etching step which influences lateral etching of the hard mask layer. One who is skilled in the art would be motivated to select an etching composition that produces the desired angle range, such as altering Liu's first etching step to produce a smooth hard mask layer sidewall.

9. As to claim 12, Liu discloses that the step of etching the bottom portion of the hard mask opening comprises the steps of: etching through a nitride layer (606) of the hard mask layer (column 11, lines 26-27, lines 45-60; column 2, lines 23-26; Figure 6); then etching through an oxide layer (604) of the hard mask layer (column 11, lines 27-

28, lines 45-60; column 2, lines 23-26; Figure 6); and then etching through a portion of the semiconductor substrate (column 11, lines 59-67; column 2, lines 26-29).

10. As to claim 13, Liu discloses that the step of etching a top portion of the hard mask opening in a BSG layer (608) (column 11, lines 24-25) and an ARC layer (column 1, lines 47-49), wherein the top portion is above the bottom portion (Figure 6).

11. As to claim 14, Liu discloses a method for forming a semiconductor structure, the method comprising the steps of: (a) providing a semiconductor substrate (602) (column 11, line 30; Figure 6); (b) forming a hard mask layer (608/606/604) on top of the semiconductor substrate (602) (column 11, lines 24-27); (c) etching a hard mask opening in the hard mask layer so as to expose the semiconductor substrate to the atmosphere through the hard mask layer opening (column 11, lines 45-60; column 2, lines 23-26), and (d) etching a deep trench in the substrate via the hard mask opening (column 11, lines 59-67; column 2, lines 26-29).

12. Liu does not expressly disclose that the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening such that a side wall of the bottom portion of the hard mask opening is substantially vertical. However, Liu teaches that the lateral etching of the overlying hard mask layers can cause the taper of the trench to deviate from the specified angle range (column 8, lines 47-54). Liu's first etching step is directed at protecting the hard mask layer during patterning (column 2, lines 26-29). Furthermore, Flander teaches that faceting on the walls of hard mask layer (104) can result in an undesirable enlargement of the trench to be etched (column 4, lines 47-60; Figure 4). Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to include the step of etching the hard mask opening comprises the step of etching a bottom portion of the hard mask opening such that a side wall of the bottom portion of the hard mask opening is substantially vertical. One who is skilled in the art would be motivated to select an etching composition that produces the desired angle range, such as altering Liu's first etching step to produce a smooth hard mask layer sidewall.

13. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liu, in view of Flander, in further view of Wolf et al., *Silicon Processing for the VLSI Era*, Vol. 1, Lattice Press (1986).

14. As to claim 15, Liu does not expressly discloses a de-polymerization step so as to remove polymers from a surface of the semiconductor structure after the step of etching the hard mask opening and before the step of etching the deep trench. Wolf teaches that scrupulously clean wafers are critical for obtaining high yields in semiconductor fabrication, including the removal of film contamination (pages 514-515). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a de-polymerization step so as to remove polymers from a surface of the semiconductor structure after the step of etching the hard mask opening and before the step of etching the deep trench. One who is skilled in the art would be motivated to maintain scrupulously clean wafers, which are critical for obtaining a high yield.

Allowable Subject Matter

15. Claims 3-11 and 16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter for claim 3: the prior art fails to teach or suggest that the second set of etching parameters are adjusted from the first set of etching parameters such that, for each trench of the second plurality of deep trenches, the step of etching the bottom portion of the hard mask opening has a lower degree of anisotropy than that associated with the a trench of the first plurality of deep trenches. The closest prior art, Liu, teaches that the lateral etching of the overlying hard mask layers can cause the taper of the trench to deviate from the specified angle range (column 8, lines 47-54), and thus teaches away from isotropic etching (or etching with a lower degree of anisotropy) of the mask layer.

17. The following is a statement of reasons for the indication of allowable subject matter for claims 6 and 17: the prior art fails to teach or suggest that the bottom portion of the hard mask opening has a greater lateral width than a top portion of the hard mask opening. The closest prior art, Liu, suggests that the hard mask opening is either uniform (Figures 5-6) or that the top portion of the hard mask opening has a greater lateral width than a bottom portion of the hard mask opening (Figures 3-4).

18. The following is a statement of reasons for the indication of allowable subject matter for claim 7: the prior art fails to teach or suggest wherein, in the formation of the first plurality of deep trenches, a first side wall of the bottom portion of the hard mask

opening associated with the nitride layer has a first height, wherein, in the formation of the second plurality of deep trenches, a second side wall of the bottom portion of the hard mask opening associated with the nitride layer has a second height, and wherein the first height is greater than the second height. The closest prior art, Liu, teaches a silicon nitride layer of a single thickness of 2,200 Å (column 11, line 27). However, there is no motivation or suggestion of varying the thickness of the silicon nitride layer.

19. The following is a statement of reasons for the indication of allowable subject matter for claim 16: the prior art fails to teach or suggest that the step of etching the bottom portion of the hard mask opening has a degree of anisotropy lower than a predetermined degree of anisotropy associated with a side wall angle which is considered substantially vertical. The closest prior art, Liu, teaches that the lateral etching of the overlying hard mask layers can cause the taper of the trench to deviate from the specified angle range (column 8, lines 47-54), and thus teaches away from isotropic etching (or etching with a lower degree of anisotropy) of the mask layer.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jain et al. (U.S. Patent No. 6,180,533) and Wang et al. (U.S. Patent No. 6,127,287) disclose plasma etching a deep trench with a silicon nitride and silicon oxide hard mask. Sundt et al. (U.S. Patent No. 6,727,158) discloses a silicon nitride and silicon oxide structure, in which the nitride is subjected to an isotropic etch to create undercutting.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
Aug. 19, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER